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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,546	10/23/2003	John R. Chase	ALTRP098/A1185	3624

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EXAMINER	
LO, SUZANNE	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,546	CHASE, JOHN R.	
	Examiner	Art Unit	
	Suzanne Lo	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/23/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/23/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 have been presented for examination.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 05/23/2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS as to the merits.

Claim Objections

MPEP 608 states:
608.01(m) [R-3] Form of Claims
The claim or claims must commence on a separate physical sheet or electronic page and should appear after the detailed description of the invention. Any sheet including a claim or portion of a claim may not contain any other parts of the application or other material. While there is no set statutory form for claims, the present Office practice is to insist that each claim must be the object of a sentence starting with "I (or we) claim," "The invention claimed is" (or the equivalent). If, at the time of allowance, the quoted terminology is not present, it is inserted by the Office of Patent Publication. Each claim begins with a capital letter and ends with a period. Periods may not be used elsewhere in the claims except for abbreviations. See Fressola v. Manbeck, 36 USPQ2d 1211 (D.D.C. 1995). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation, 37 CFR 1.75(i).

3. Claims 5, 13, 21 is objected to because of the following informalities:

In claims 5 and 21, the word "place" is misspelled as "plrace".

In claim 13, the word "width" is misspelled as "sidth". Appropriate correction is required.

4. Claim 10 is objected to because it fails to comply with 37 CFR 1.75(i) by missing the period.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1-27 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Specifically, claims 1-16 are software *per se*, which is abstract. Claims including the limitation of a computerized method are written so broadly they do not have to include hardware, only software. According to these claims, a computerized method is not necessarily embodied in hardware.

Specifically, claims 1-27 do not produce a tangible result. The claims do not enable their usefulness to be realized, the claims only generate, instantiate, parameterize, and provide logic and there is no tangible output. The broadest reasonable interpretation of generating a test design is not necessarily displaying or saving the design to a file and can just be computation of the test design.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "substantial" in claims 1, 17, and 25 is a relative term which renders the claims indefinite. The term "substantial" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim 10 is rejected under 35 U.S.C. 112, second paragraph, for failing to further narrow claim 8 which it is dependent on.

Claim 12 recites the limitation "wherein generating randomized logic" in the first two lines of the claim. There is insufficient antecedent basis for this limitation in the claim.

All other claims not specifically treated are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. **Claims 1-13 and 17-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Zaidi et al. (U.S. Patent Application Publication 2002/0038401 A1) in view of Heinkel et al. (U.S. Patent Application Publication 2004/0015739 A1).**

As per claim 1, Zaidi is directed to a computerized method for generating a testbench **([0029]-[0032])**, the method comprising: a plurality of test designs **([0037])**, the plurality of test designs having varied characteristics **([0054])** to allow substantial testing of a design automation tool, wherein generating one of the plurality of test designs comprises: instantiating the I/O structure of a top level module, the top level module having input and output pins **([0048]-[0052])**; parameterizing a plurality of submodules from a design module library for

interconnection with the top level module, the plurality of submodules having input and output lines **([0039, Table 1])**; providing logic to interconnect the plurality of parameterized submodules as well as to connect the plurality of parameterized submodules to various input and output pins of the top level module **([0050])** but fails to specifically disclose generating a plurality of test designs.

Heinkel teaches generating a plurality of test designs **([0057]-[0060])** Zaidi and Heinkel are analogous art because they are from the same field of endeavor, validating an IC with a testbench. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of validating an IC of Zaidi with the method of generating test designs of Heinkel in order to allow testing of different designs without needing to recompile the VHDL testbench for each test design **(Heinkel, [0058])**.

As per claim 2, the combination of Zaidi and Heinkel already discloses the computerized method of claim 1, wherein the design automation tool is used to implement hardware descriptor language designs on a programmable chip **(Zaidi, [0031])**.

As per claim 3, the combination of Zaidi and Heinkel already discloses the computerized method of claim 1, wherein the design automation tool is used to implement designs on an ASIC **(Zaidi, [0029])**.

As per claim 4, the combination of Zaidi and Heinkel already discloses the computerized method of claim 1, wherein the design automation tool is an electronic design automation tool **(Zaidi, [0025], [0032])**.

As per claim 5, the combination of Zaidi and Heinkel already discloses the computerized method of claim 1, wherein the design automation tool is a synthesis or a plrace and route tool **(Zaidi, [0032])**.

As per claim 6, the combination of Zaidi and Heinkel already discloses the computerized method of claim 1, wherein providing logic to interconnect the plurality of parameterized modules comprises identifying inputs and outputs **(Zaidi, [0048]-[0060])**.

As per claim 7, the combination of Zaidi and Heinkel already discloses the computerized method of claim 6, wherein inputs comprise input pins of the top level module, submodule output lines, and registers **(Zaidi, [0048]-[0060])**.

As per claim 8, the combination of Zaidi and Heinkel already discloses the computerized method of claim 6, wherein outputs comprise output pins of the top level module, submodule input lines, and registers **(Zaidi, [0048]-[0060])**.

As per claim 9, the combination of Zaidi and Heinkel already discloses the computerized method of claim 8, wherein providing logic to interconnect the plurality of parameterzied modules but does not disclose classifying inputs and outputs as clock lines, control lines, and data lines. Official notice is taken with respect to this limitation. Specifically it would have been obvious to one of ordinary skill in the art at the time of Applicants invention to have this feature in order to prevent errors when interconnecting inputs and outputs.

As per claim 10, the combination of Zaidi and Heinkel already discloses the computerized method of claim 8, wherein generating one of the plurality of test designs further comprises: **(Zaidi, [0048]-[0060])**

As per claim 11, the combination of Zaidi and Heinkel already discloses the computerized method of claim 10, generating randomized logic to drive outputs **(Zaidi, [0047])**.

As per claim 12, the combination of Zaidi and Heinkel already discloses the computerized method of claim 10, wherein generating randomized logic comprises directly wiring outputs to inputs, generating a logic expression using inputs, generating a mathematical expression using inputs, or generating decision logic **(Zaidi, [0047])**.

As per claim 13, the combination of Zaidi and Heinkel already discloses the computerized method of claim 6, but fails to disclose wherein parameterizing the plurality of submodules comprises defining interfaces, data sidth, and the type of signal for input and output lines associated with the

submodule. Official notice is taken with respect to this limitation. Specifically it would have been obvious to one of ordinary skill in the art at the time of Applicants invention to have this feature in order to prevent errors when interconnecting inputs and outputs.

As per claim 15, the combination of Zaidi and Heinkel already discloses the computerized method of claim 6, wherein generating one of the plurality of test design further comprises selecting a clock structure for each output **(Zaidi, [0047])**.

As per claims 17-24, Zaidi discloses a computer system for generating a testbench **([0029]-[0032])**, the computer system comprising: memory operable to hold information associated with a design module library **([0025])**, a processor coupled to memory **([0025])**, the processor configured to execute a method with the same limitations of claim 1 and is therefore rejected over the same art combination.

As per claim 25-27, Zaidi is directed to an apparatus for generating test a testbench **([0029]-[0032])**, the apparatus comprising: means for a method with the limitations of claim 1 and is therefore rejected over the same art combination.

8. **Claims 14 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaidi et al. (U.S. Patent Application Publication 2002/0038401 A1) and Heinkel et al. (U.S. Patent Application Publication 2004/0015739 A1) **in further view of Goossens ("Design of Heterogeneous ICs for Mobile and Personal Communication Systems").**

As per claim.14, the combination of Zaidi and Heinkel is directed to the computerized method of claim 6, wherein submodules comprise memory and timers **([0037])** but fails to disclose wherein submodules comprise adders and phase lock loops. Goossens teaches submodules comprising of adders and phase lock loops **(page 524-525, Figure 1, Section 3.2)**. Zaidi, Heinkel, and Goossens are analogous art because they are all from the same field of endeavor, validating an IC. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of validating an IC with

a testbench of Zaidi and Heinkel with the adders and phase lock loops of Goossens in order to allow the design of heterogeneous IC architecture **(page 524, Section 1)**.

As per claim 16, the combination of Zaidi and Heinkel is directed to the computerized method of claim 15, but fails to specifically disclose wherein clock structures include a plurality of synchronous and asynchronous structures. Goossens teaches clock structures that include a plurality of synchronous and asynchronous structures **(page 525-526, Section 3.3)**. Zaidi, Heinkel, and Goossens are analogous art because they are all from the same field of endeavor, validating an IC. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of validating an IC with a testbench of Zaidi and Heinkel with the clock structures of Goossens in order to implement handshaking, protocol control, and synchronization functionalities for heterogeneous IC architecture **(page 525-526, Section 3.3)**.

Conclusion

9. The prior art made of record is not relied upon because it is cumulative to the applied rejection. These references include:

1. U.S. Patent No. 6,477,691 B1 issued to Bergamashi/Rab et al. on 11/05/02.
2. U.S. Patent Application Publication No. 2004/0015792 A1 published by Kubista on 01/22/04.
3. U.S. Patent No. 6,053,947 issued to Parson on 04/25/00.
4. "ASIC to FPGA Design Methodology & Guidelines" published by Altera in July 2003.

10. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suzanne Lo
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SL
03/14/06

KAMINI SHAH
SUPERVISORY PATENT EXAMINER